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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,232	08/24/2001	William Joseph Armstrong	IBM / 182	4082

26517 7590 03/09/2005

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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,232	ARMSTRONG ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were previously presented for examination and rejected. Claims 6, 8, 9, 15, 17, and 18 have been amended. New claim 21 has been added. Claims 1-21 have been submitted for examination. Claims 1-21 have been rejected.

Drawing Objections

The Examiner thanks Applicant for amending the drawings. Those objections have been withdrawn. The Examiner concurs that no new matter has been added.

Claim Rejections – 35 U.S.C. § 112

The Examiner thanks Applicant for amending the claims to overcome the previous rejections under 35 U.S.C. § 112, second paragraph. Those rejections have been withdrawn.

Claim Rejections – 35 U.S.C. § 102

The Examiner apologizes for the ambiguity in the previous office action regarding which claims were rejected as being anticipated by US Patent No. 5,872,963 to Bitar et al. (Bitar). Applicant was correct in presuming that claims 1-20 were rejected.

Regarding the interpretation of Bitar and as applied to claim 1, Applicant argues:

> Bitar et al. distinguishes between virtual processors and threads at col. 1, lines 27-33. Fig. 2b of Bitar et al. further illustrates this distinction in showing threads 2 mapped to kernel space comprising virtual processors 5 (col. 5, lines 64-65). Fig. 8 likewise shows threads 24.M switched without using kernel space 18 (and associated virtual processors 45). Because Bitar et al. at

> least fails to teach or suggest the virtual processor feature of claim 1, claim 1 is novel and non-obvious over the cited prior art.
> Moreover, Bitar et al. fails to suggest or motivate the features of claim 1, including switching-in a virtual processor. In fact, Bitar et al. teaches away from using a virtual processor, or kernel, and associated scheduling during thread switching for efficiency reasons (col 5, lines 14-18 and col. 12, line 24).

The Examiner respectfully traverses this argument as follows:

The Examiner disagrees with this interpretation of Bitar. Where Bitar distinguishes between virtual processors and threads, Bitar also states (column 1, lines 34-39; emphasis added):

> **A virtual processor may be** a process, such as that provided by traditional UNIX systems, **a kernel thread**, such as that provided by Mach, or some other abstraction. It is the definition of the virtual processor and the related mapping of user-level threads to virtual processors that defines the performance characteristics of a threads implementation.

Although Bitar teaches an embodiment concerning user-threads, this is exemplary of the broader concept of *execution entities* (abstract). Bitar then proceeds to define the term *virtual processor* (column 1, line 54 – column 2, line 5, emphasis added).

> Virtual Processors
> **Every operating system exports an abstraction that represents the basic unit of scheduling.** Under UNIX, for example, the process is the fundamental abstraction that is scheduled; **under Mach the kernel thread is the equivalent entity. This abstraction, a virtual processor, is scheduled by the operating system scheduler for execution on available physical processors.** It is called a virtual processor because an application may treat it as a processing resource independent of whether it is "backed" by a physical processor.
> A traditional UNIX process cannot execute in parallel on a multiprocessor precisely because **a virtual processor is a process** (a single virtual processor can only be scheduled onto a single physical processor); multiple processes can run concurrently, but if there is only a single runnable process all the processors but one will be idle. A Mach process having multiple kernel threads can run concurrently on multiple processors since **the virtual processor is a kernel thread** and the process may be comprised of multiple kernel threads.

It is clear from this that Bitar discloses the synonymous definitions of "process", "thread", and "virtual processor" as known in the art. Regarding the distinction between user level threads and kernel level threads, Applicant has failed to prove a patentable distinction between an invention regarding one or the other. In practice, the distinction

is largely one of scope. User threads are often grouped to execute on a kernel thread (an execution entity), and kernel threads are grouped to execute on a processor (an execution entity). The same issues of scheduling, including yielding, blocking, race conditions, and deadlocks are well known to be applicable to either type of thread. Further, the arrangement of user and kernel threads has long been known in the art.

Regarding Applicant's allegation that Bitar teaches away from scheduling a virtual processor, Bitar does not teach away from scheduling a virtual processor because of technical issues pertinent to the disclosed invention, but rather discloses that the *performance characteristics of the thread implementation* are defined by the definition of the virtual processor (column 5, lines 14-18). At the second citation (column 12, line 24) Bitar discloses that when switching *user* threads, efficiency dictates that this operation not involve the kernel. Bitar does not teach that switching *kernel threads*, "virtual processors", is an inefficient or unusable process.

The Examiner finds Applicant's arguments regarding the definition of "thread" versus "virtual processor" to be neither persuasive nor patentably distinct. Therefore, the Examiner maintains the previous rejections under 35 U.S.C. § 102(b) based on Bitar.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21 are rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,872,963 to Bitar et al. (Bitar).

1. Regarding claim 1, Bitar et al. teaches a system and method for context switching between a first and a second execution entity (abstract) wherein

the system supports a plurality of partitions (column 6, line 9-11; Fig 10),

the partitions include a plurality of virtual processors that share at least one CPU (column 8, line 21-54; column 15, lines 34-45),

requesting with a yielding virtual processor a yield of the CPU upon which the virtual processor is executing including designating a target virtual processor from among the plurality of virtual processors (column 10, line 48 – column 11, line 10), and

switching-in the target virtual processor for execution by the CPU in response to the requested yield (column 10, lines 20-33; column 11, lines 33-41).

Although Bitar et al. teaches the invention in terms of threads, the same method can be used to switch between other types of execution entities (column 13, lines 49-52).

2. Regarding claim 2, Bitar et al. teaches a method of context switching wherein the target virtual processor requires access to the CPU, wherein the yielding virtual processor controls the CPU (column 10, line 48 – column 11, line 10; column 11, lines 33-41).

3. Regarding claim 3, Bitar et al. teaches a method of context switching comprising generating a yield command from the virtual processor, wherein the yield command includes pointer and status information regarding the target virtual processor (column 10, lines 9-33).

4. Regarding claim 4, Bitar et al. teaches a method of context switching comprising assigning status information to the target virtual processor (column 10, lines 9-33).

5. Regarding claim 5, Bitar et al. teaches a method of context switching comprising assigning a target count to the target virtual processor (column 10, lines 9-33). The preempt bit vector holds a value of 0 for a thread that has its resource requirements fulfilled and holds a value of 1 for a thread that has been preempted and requires resources to continue.

6. Regarding claim 6, Bitar et al. teaches a method of context switching comprising comparing the target count to a presented count conveyed in the yield request (column 10, lines 9-33; column 13, line 53 – column 14, line 24; column 16, lines 29-44).

7. Regarding claim 7, Bitar et al. teaches a method of context switching comprising aborting the yield in response to a yield-to-active command. If the processor is not needed, it will be reallocated to another process (column 16, lines 29-44).

8. Regarding claim 8, Bitar et al. teaches a method of context switching comprising designating the yielding virtual processor as waiting for the target virtual processor (column 10, line 48 – column 11, line 10; column 11, lines 33-41; column 16, lines 29-44).

9. Regarding claim 9, Bitar et al. teaches a method of context switching comprising designating the target virtual processor as having a yielding processor waiting for the target virtual processor (column 13, line 53 – column 14, line 24; column 16, lines 29-44).

10. Regarding claim 10, Bitar et al. teaches a method of context switching comprising storing the state of the yielding virtual processor (column 10, lines 9-33; column 13, lines 53-60).

11. Claims 11-18 are directed toward an apparatus comprising a computer system and a computer program to execute the method of claims 1-3, and 5-9. As the invention of Bitar et al. is a computer system and program (abstract), claims 11-18 are rejected for reasons similar to those given for claims 1-3, and 5-9 above.

12. Claims 19 and 20 are directed toward a program product and signal bearing medium bearing a computer program which executes the method of claim 1. As the invention of Bitar et al. can be realized with a computer program, whether transmitted via a network or stored locally (abstract; column 17, lines 20-27; column 20, line 49 – column 21, line 10), claims 19 and 20 are rejected for reasons similar to those given for claim 1 above.

13. Regarding claim 21, Bitar teaches a user-level scheduler which includes a queue (schedule) used to schedule ready-to-run threads (column 8, lines 21-31). It is inherent that a user-level scheduler is a thread, therefore a virtual processor.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

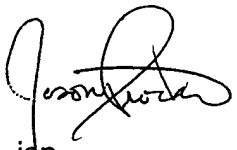
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Jason Proctor
Examiner
Art Unit 2123